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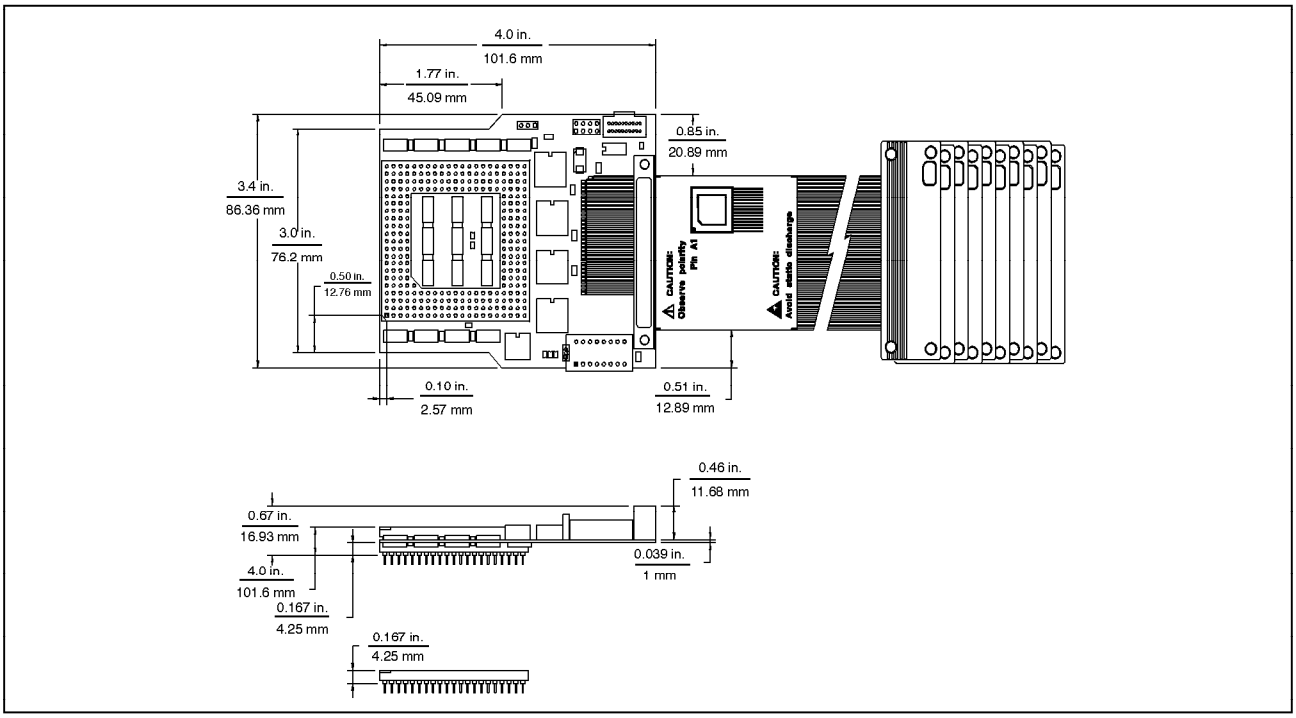
HP E2443B

Preprocessor Interface for Intel Pentium™ Processor at iCOMP* Index 510\60 MHz and 567\66 MHz

For use with HP logic analyzers

The HP E2443B preprocessor interface for the Intel Pentium processor 510\60 MHz (567\66 MHz) allows you to easily connect an HP logic analyzer to your target system. The preprocessor has four modes of operation. In state-per-transfer mode, the logic analyzer is clocked upon completing data transfer cycles. In this mode, the preprocessor keeps track of the address pipeline and aligns data with its parent address. Additionally, activity during an HLDA or BOFF# assertion is captured. In the second mode of operation, state-per-clock mode, data is captured on every system clock, so you see all processor activity including wait and idle states. This mode of operation is useful in finding memory locations that do not respond with data and in checking memory control systems.

In the third mode of operation, timing analysis, all signals are buffered, but otherwise pass straight through to the logic analyzer In the fourth mode of operation, the debugger mode, it is identical to state-per-transfer mode, with the exception that whenever IU, IV, or IBT are asserted, data is captured regardless of whether or not it is valid.



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Software is included with the HP E2443B that automatically configures the logic analyzer, labeling address, data, and status lines. Additionally, an inverse assembler displays execution traces in Intel Pentium microprocessor mnemonics.

Microprocessor Supported
273-pin PGA package for Intel Pentium processor 510\60 MHz (567\66 MHz) CPU.

Capabilities
- The locic analyzer captures all bus cycles, including prefetches. Unexecuted prefetches are marked.
- Disassembly of floating point instructions is supported.
- Burst mode addresses are calculated and displayed in the state trace listing.
- Timing analysis is supported. All signals go through 6.3-ns maximum buffers (P/N 74FCT646AT).
- State-per-clock mode runs up to 100 MHz providing margin for testing.
- Preprocessor can be configured to prequalify the logic analyzer clock on BRDY#, ADS#, EADS#, BOFF#, HLDA saving logic analyzer resources.

Logic Analyzers Supported
Two-card HP 16550A, or four-card HP 16540 and 16541 (A and D models). Both of these analyzers plug into the HP 16500A mainframe. In addition, the HP 1660A is supported for inverse assembly.

Pods Required
Eight 16-channel pods are required for inverse assembly. Two additional pods provide monitoring of other status signals.

Termination Adapters (TA)
All ten pods are terminated on the preprocessor. No additional TAs are required.

Maximum Clock Speed
66 MHz

Probe Loading
- 7 pF in series with 100 Ω on CLK.
- 14 pF in series with 50 Ω on ADS#, BOFF#, BRDY#, BRDYC#, HLDA, KEN#, W/R#.
- 14 pF on IU, IV, IBT, INIT, TCDO, SMIACT#, R/S# and RESET.
- 10 pF on all other signals.

For more information, call your local HP sales office listed in your telephone directory, or an HP regional office listed below for the location of your nearest sales office.

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